Abstract of the Disclosure

A semiconductor device in which a silica aerogel layer having a very low dielectric constant is used as an insulating layer such that parasitic capacitance between a gate electrode and a source electrode in a field effect transistor having a T-shaped gate electrode, and a method of manufacturing the same are provided. The semiconductor device includes a semiconductor substrate, source and drain electrodes, which are formed on the semiconductor substrate to make ohmic contact with the semiconductor substrate, a T-shaped gate electrode, which is formed between the source and drain electrodes on the semiconductor substrate, and an insulating layer including a silica aerogel layer, the silica aerogel layer being interposed between the gate electrode and the source and drain electrodes.